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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/550,241 | 09/23/2005 | Sven Mattison | P17211-US2 | 1739 |

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| EXAMINER | |
|---|---|
| GOODLEY, JAMES E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2817 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/550,241 | MATTISON, SVEN | |
| | Examiner | Art Unit | |
| | JAMES E. GOODLEY | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4 and 6-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments filed 4/16/2008 have been fully considered but are moot in view of the new grounds of rejection set forth herein, being necessitated by amendment.

The double patenting rejection is removed, as applicant has submitted a valid terminal disclaimer.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Sauer (US 6,064,257 – of record)*** in view of ***Bezhad (US 6,759,904)***.

Regarding **claims 1-4, 6-8 and 14-20,** Figs 5-7 of Sauer disclose a device for generating a random sequence of bits, comprising;

oscillating means [VCO/CCO 62] having an input terminal for receiving a bias as input, the oscillating means comprising at least one oscillator amplifier [Q17-Q30];

amplifier means [Q15-Q30] comprising the at least one oscillator amplifier and a corresponding at least one differential amplifier [Q15 and Q16] coupled to the at least one oscillator amplifier.

The input bias terminal is coupled to a noise source [50] for generating intrinsic noise, the noise source comprising a noisy amplifier cell having amplifying means [G1-G4], a load [Q7-Q12] coupled to the amplifying means and supply, and a tail current source [I1-I4] coupled to grounding means and the amplifying means.

Sauer, fails to disclose a load further comprising cascoded transistors coupled to the amplifying means.

However, Fig. 15 of Bezhad discloses a conventional differential common-source, cascode amplifier, with transistors 1590 and 1592 cascoded with input transistors 1584 and 1586. The amplifier further includes a tail current source [1588] and a common mode feedback circuit [1480].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Sauer to utilize a conventional differential cascode amplifier, such as that disclosed by Bezhad, for the purpose of ensuring a higher slew rate output.

Regarding **claim 9**, Sauer in view of Bezhad discloses the device of claim 1, but fails to disclose, "wherein the cascode transistors, the amplifying means, and the tail current source of the noisy amplifier cell comprises BJT (Bipolar Junction Transistors) transistors."

However, one of ordinary skill in the art would recognize that BJT transistor implementation is an equivalency of using MOS transistor technology.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Sauer in view of Bezhad to utilize bipolar

transistor technology instead of the MOS technology disclosed in Sauer in view of Bezhad, as such implementation is an art-recognized equivalency and exhibits better high frequency performance.

Regarding **claims 10 and 11**, Sauer in view of Bezhad discloses the device of claim 1, but fails to disclose, "wherein the cascoded transistors comprise PMOS [or NMOS] transistors and the amplifying means and tail current source comprises NMOS [or PMOS] transistors."

However, one of ordinary skill in the art would recognize that the NMOS topology in Sauer in view of Bezhad could equivalently be adapted to implementation with an NMOS load and PMOS tail current source (or vice versa).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Sauer in view of Bezhad to utilize an NMOS load and PMOS tail current source (or vice versa), as such an implementation is the functional equivalent of the PMOS load and NMOS tail current source.

Regarding **claim 12**, the device of Sauer in view of Bezhad fails to disclose the device according to claims 10 and 11, "wherein the width-over-length ratio of the transistors of the amplifying means is at least 3 times the width-over-length ratio of the transistors of the tail-current source, and the width-over-length ratio of the second transistor pair of the load is at least 3 times the size of the width-over-length ratio of the first transistor pair of the load."

However, there appears to be no criticality in the applicant's disclosure as to the particular width-length ratio of the transistors. It is believed the ratio is simply a design choice for one of ordinary skill in the art to decide upon.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Sauer in view of Bezhad to utilize the particular width to length ratio of the claimed transistors, as such transistor sizes are a mere design choice.

Regarding **claim 13**, the device of Sauer in view of Bezhad fails to disclose the device according to claim 12 wherein the width of the transistors of the amplifying means and the transistors of the second transistor pair of the load is in the range of 2.5-125 .mu.m, and the length of the transistors is in the range of 0.25-12.5 .mu.m; the width and the length of the transistors of the tail-current source and the transistors of the first transistor pair of the load are in the range of 0.25-12.5 .mu.m.

However, there appears to be no criticality in the applicant's disclosure as to the particular width-length ratio of the transistors. It is believed the ratio is simply a design choice for one of ordinary skill in the art to decide upon.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Sauer in view of Bezhad to utilize the particular width to length ratio of the claimed transistors, as such transistor sizes are a mere design choice.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES E. GOODLEY whose telephone number is (571)272-8598. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/James E Goodley/

Examiner, Art Unit 2817

/Robert Pascal/

Supervisory Patent Examiner, Art Unit 2817